Session 28 Overview

Wireline Building Blocks

Chair: Kevin Kornegay, Georgia Institute of Technology, Atlanta, GA

Associate Chair: Herman Casier, AMI Semiconductors, Oudenaarde, Belgium

This session addresses the key issues associated with the design of building blocks to facilitate advances in wireline communications.

Size reduction is an important factor in increasing the line densities in telephone exchanges. Paper 28.1 employs a selectivity booster chip and compact LC low-pass filter to replace the bulky POTS/ADSL splitter.

To meet the performance demands of future high-data-rate communication systems requires high-frequency amplifiers with high gain and large bandwidth. Implementation in CMOS is essential in reducing the cost of the components that make up these systems. In paper 28.2 traditional shunt and series inductive peaking are combined with capacitive bandwidth extension to achieve 44GHz bandwidth with a 19dB gain in 90nm CMOS. Paper 28.3 presents design techniques for an AGC amplifier to accommodate a 35dB dynamic range input signal level at 10Gb/s data rate. The 0.18μm CMOS chip incorporates a peak detector, integrator, and exponential voltage generator in the gain control loop. Paper 28.9 achieves 20Gb/s data demultiplexing in a 0.13μm CMOS technology. A very compact circuit is realized by avoiding the use of inductors.

Bidirectional signaling allows for doubling data capacity of a single twisted-pair line. Paper 28.4 presents a 0.11μm CMOS chip that reaches a maximum data rate per differential pair of 20Gb/s using a resistor-transconductor hybrid circuit for the upstream and downstream signals.

Timing accuracy is a basic challenge in high-speed electrical communication links. The following papers describe advances in clock-jitter measurements, clock duty-cycle control, and clock generation. Paper 28.5 uses an oversampling technique in an on-chip jitter measurement macro to achieve 1ps of resolution. Paper 28.6 presents a high-precision arbitrary timing generator for ATE applications with 40 channels available at 1GHz or 10 multiplexed channels at 4GHz, each with a timing resolution of 1.83ps. Paper 28.7 describes a clock duty-cycle IC capable of correcting a 50 ±20% clock signal duty-cycle to a 1.25% accurate user selectable duty-cycle.

Process variability has a tremendous impact in maintaining circuit performance. Paper 28.8 demonstrates 66GHz divider operation in 90nm SOI CMOS using a statistical methodology and proves its manufacturability against process variability with comprehensive characterization data.

To support future high-data-rate communications very high-speed PRBS pattern generators are required. Paper 28.10 sets a speed record for on-chip PRBS generation using an advanced InP DHBT technology.

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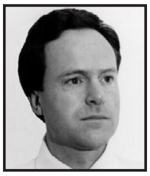


28.1 A 5V AC-Powered CMOS Filter-Selectivity Booster for POTS/ADSL Splitter Size Reduction **8:30 AM**

E. Sackinger, Conexant Systems, Red Bank, NJ

A 0.5µm CMOS chip contains a 5th-order continuous-time filter, a low output-impedance driver, and an active rectifier. The chip boosts the selectivity of an external passive LC LPF and achieves an ADSL isolation of 70dB at 30kHz, while maintaining a passband flatness of 0.23dB. It consumes 35mW from a 5V supply and reduces the number of transformers and the size of POTS/ADSL splitters.

28.2 A DC-to-44GHz 19dB Gain Amplifier in 90nm CMOS Using Capacitive Bandwidth Enhancement **9:00 AM**

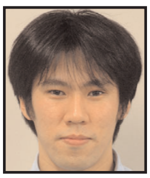
J. Weiss, IBM, Rüschlikon, Switzerland

A dc-to-44GHz amplifier with 19dB differential gain in a standard 90nm CMOS technology is presented. Capacitive bandwidth and group-delay enhancements are combined with series peaking in a shunt-peaking amplifier. The circuit occupies 0.02mm^2 and dissipates 57mW at 1V.

28.3 A 10Gb/s CMOS AGC Amplifier with 35dB Dynamic Range for 10Gb Ethernet **9:30 AM**

C-F. Liao, National Taiwan University, Taipei, Taiwan

A 10Gb/s AGC amplifier is implemented in 0.18µm CMOS technology. The circuit uses a linear-in-dB controlled VGA with 58dB tuning range. For input swings from 18mV$_{pp}$ to 1V$_{pp}$, the output swing is 430mV$_{pp}$ within +0.4 to -0.8dB variations. The measured dynamic range is 35dB with BER <10^{-12}. The AGC consumes 54mW from a 1.8V supply.



28.4 A 20Gb/s Bidirectional Transceiver Using a Resistor-Transconductor Hybrid **9:45 AM**

Y. Tomita, Keio University, Yokohama, Japan

A 20Gb/s simultaneous bidirectional transceiver uses a resistor-transconductor hybrid in a standard 0.11µm CMOS process. The 7mW hybrid works in a continuous-time domain without any replica driver and eliminates the need for the precise matching between the replica- and main-driver characteristics.

28.5 A 1ps-Resolution Jitter-Measurement Macro Using Interpolated Jitter Oversampling **10:15 AM**

K. Nose, NEC, Kanagawa, Japan

An in-field real-time successive jitter-measurement macro is developed. It features interpolated jitter oversampling and feedforward calibration that help attain 1ps resolution and a hierarchical vernier jitter-measurement technique that exploits the trade-off between rms and deterministic jitter measurement characteristics.

28.6 1.83ps-Resolution CMOS Dynamic Arbitrary Timing Generator for >4GHz ATE Applications **10:45 AM**

T. Okayasu, Advantest, Gunma, Japan

A high-speed high-precision dynamic arbitrary timing generator, fabricated in a 0.18µm CMOS process, for >4GHz ATE applications is demonstrated. It exhibits a maximum operating frequency of 1.066 and 4.266GHz (multiplexed mode), a timing resolution of 1.83ps, an INL of <±4ps excluding the calibration RAM, and a random jitter of <0.7ps$_{rms}$.

28.7 A Clock Duty-Cycle Correction and Adjustment Circuit **11:15 AM**

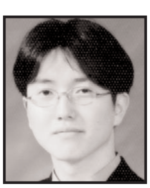
J. S. Humble, Mayo Clinic, Rochester, MN

A clock duty-cycle correction circuit that accepts input duty cycles ranging from 30% to 70% and maintains a user-selectable output duty cycle over a frequency range of 500MHz to 6GHz is demonstrated. The output duty cycle is selectable from 41.25% to 58.75% in 1.25% increments. The circuitry is integrated into a clock-distribution chip which provides 10 identical outputs.

28.8 Performance Variations of a 66GHz Static CML Divider in 90nm CMOS **11:30 AM**

J-O. Plouchart, IBM, Hopewell Junction, NY

A 66GHz maximum operating clock frequency is measured for a 90nm CMOS static CML divide-by-2 with a 25.5mW latch power dissipation. Statistical self-oscillation frequency measurements exhibit a mean of 42.6 and 39.2GHz at 25°C and 85°C, and a 2.8GHz standard deviation. The mean dissipated power is 44.3mW at 1.4V, with a 2.2mW standard deviation.



28.9 A 20Gb/s 1:4 DEMUX Without Inductors in 0.13µm CMOS **11:45 PM**

B-G. Kim, KAIST, Daejeon, Korea

A 20Gb/s 1:4 DEMUX is implemented in a 0.13µm CMOS technology. The chip has no inductors and features a coupled latch with shared-current-source and buffer-insertion scheme, a divide-by-2 circuit with a static frequency divider, and a DLL. The measured eye-opening width and height are 71.3% and 52%, respectively. The 1.05×0.92mm^2 chip consumes 210mW from a 1.2V supply.

28.10 104Gb/s 2^{11}-1 and 110Gb/s 2^9-1 PRBS Generator in InP HBT Technology **12:00 AM**

T. Kjellberg, Chalmers University of Technology, Göteborg, Sweden

A 2^{11}-1 PRBS generator with one output at a maximum data rate of 104Gb/s and 4 parallel outputs at 52Gb/s is presented together with a 2^9-1 PRBS generator with a single output at 110Gb/s. The ICs are implemented in a 300GHz f$_T$ InP HBT technology. The generator core is clocked at half the data rate of the high-speed output for both circuits. They dissipate 2.8W and 2.2W from a -3.5V supply, respectively.